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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,917	10/30/2003	Chris Aldridge	1415.P007US/KJT/ayu	5640

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LAWRENCE Y.D. HO & ASSOCIATES PTE LTD
30 BIDEFORD ROAD, #02-02, THONGSIA BUILDING
SINGAPORE, 229922
SINGAPORE

EXAMINER	
PHU, PHUONG M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,917	ALDRIDGE ET AL.	
	Examiner	Art Unit	
	Phuong Phu	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,23 and 27-30* is/are rejected.

7)☒ Claim(s) *16-22 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-15, 23 and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Black et al (6,738,608).

-Regarding to claim 1, see figures 1, 2 and 4, and col. 3, line 2 to col. 7, line 65, col. 4, line 36 to col. 14, line 53, Black et al discloses a control signal generating circuit (400) (see

figure 4) for an automatic frequency control (AFC) circuit (130a) (see figure 2), the control signal generating circuit comprising:

an input (input of (240a) for receiving signal (Terr) (see figure 4)) for coupling to a tracking circuit (comprising (226, 224a, 224b) (see figure 2) of the AFC circuit to receive a digital timing control signal (Terr) therefrom;

a processor (comprising (240a, 230a) (see figure 4) for receiving the digital timing control signal and producing a frequency control signal (Fctrl1); and

an output (output of (230a) (see figure 4) for coupling to a variable frequency generator (122a) of the AFC circuit to provide the frequency control signal thereto, the frequency control signal for determining output frequency of the variable frequency generator.

-Regarding to claim 2, Black et al discloses that the processor comprises an amplifier (472a) (see figure 4) coupled to receive the digital timing control signal and a predetermined amplification factor (c1), the amplifier for amplifying the digital timing control signal by the predetermined amplification factor to produce an amplified digital timing control signal, and the amplifier having an output coupled to provide the amplified digital timing control signal (see col. 13, lines 37-50).

-Regarding to claim 3, Black et al discloses the processor further comprises an integrator (comprising "accumulator" (474a, 476a) (see figure 4)) having an input coupled to receive the amplified digital timing control signal, the integrator for integrating the amplified digital timing control signal for producing the frequency control signal, and the integrator having an output coupled to provide the frequency control signal (see col. 13, lines 37-50).

-Regarding to claim 4, Black et al discloses that the amplifier comprises a multiplier (472b) (see figure 4), and the predetermined amplification factor comprises a predetermined multiplication factor (c1), the multiplier for multiplying the digital timing control signal by the predetermined multiplication factor to produce a multiplied digital timing control signal, and the amplified timing control signal comprises the multiplied digital timing control signal (see col. 13, lines 37-50).

-Regarding to claim 5, Black et al discloses that the input for coupling to the tracking circuit of the AFC circuit is adapted to receive a plurality of digital outputs (on-time, early, late) (see figure 2).

-Regarding to claim 6, Black et al discloses that the input for coupling to the tracking circuit of the AFC circuit is adapted to receive at least three digital outputs (on-time, early, late), wherein the at least three digital outputs represent three different logic states (see figure 2).

-Regarding to claim 7, Black et al discloses that the input for coupling to the tracking circuit of the AFC circuit is adapted to receive three digital outputs (on-time, early, late), wherein a first of the three digital outputs indicates timing delay, wherein a second of the three digital outputs indicates timing advance, and wherein a third of the three digital outputs indicates timing remains unchanged (see figure 2).

-Regarding to claim 8, as similarly applied to claims 1-7, set forth above and herein incorporated, see figures 1, 2 and 4, and col. 3, line 2 to col. 7, line 65, col. 4, line 36 to col. 14, line 53, Black et al discloses a method (400) (see figure 4) for generating a frequency control signal (Fctrl1)) for an automatic frequency control (AFC) circuit (130a) (see figure 2), the method comprising:

procedure of (240a) (see figure 4) receiving a digital timing control signal (Terr) from a tracking circuit of the AFC circuit (comprising (226, 224a, 224b) (see figure 2);

procedure (240a, 230a) (see figure 4) of processing the digital timing control signal to produce the frequency control signal; and

procedure (230a) (see figure 4) of providing the frequency control signal to a variable frequency generator (122a) of the AFC circuit, wherein the frequency control signal determines output frequency of the variable frequency generator.

-Regarding to claim 9, as similarly applied to claim 5, Black et al discloses procedure of receiving a plurality of digital outputs (on-time, early, late) (see figure 2).

-Claim 10 is rejected with similar reasons set forth for claim 6.

-Claim 11 is rejected with similar reasons set forth for claim 7.

-Claim 12 is rejected with similar reasons set forth for claim 2.

-Claim 13 is rejected with similar reasons set forth for claim 4.

-Claim 14 is rejected with similar reasons set forth for claim 3.

-Regarding to claim 15, as similarly applied to claims 1-14, set forth above and herein incorporated, see figures 1, 2 and 4, and col. 3, line 2 to col. 7, line 65, col. 4, line 36 to col. 14, line 53, Black et al discloses a control signal generating circuit (400) (see figure 4) for an automatic frequency control (AFC) circuit (130a) (see figure 2), the control signal generating circuit comprising:

an input (input of (240a) for coupling to a tracking circuit of the AFC circuit to receive a digital timing control signal (Terr) (see figure 4)) therefrom;

a controller (inherently included as a splitter for receiving and splitting/passing portions of the digital timing control signal (Terr) to (472a, 472b) (see figure 4)) for receiving the digital timing control signal, and the controller for passing at least a portion of the digital timing control signal;

a processor (comprising (240a, 230a) (see figure 4) for receiving the at least the portion of the digital timing control signal and producing a frequency control signal (Fctrl1); and

an output (output of (230a) (see figure 4) for coupling to a variable frequency generator (122a) of the AFC circuit to provide the frequency control signal thereto, the frequency control signal for determining output frequency of the variable frequency generator.

-Regarding to claim 23, as similarly applied to claims 1-14, 15, set forth above and herein incorporated, see figures 1, 2 and 4, and col. 3, line 2 to col. 7, line 65, col. 4, line 36 to col. 14, line 53, Black et al discloses a method (400) (see figure 4) for generating a frequency control signal (Fctrl1) for an automatic frequency control (AFC) circuit(130a) (see figure 2), the method comprising:

procedure (240a) (see figure 4) of receiving a digital timing control signal (Terr) from a tracking circuit of the AFC circuit (comprising (226, 224a, 224b) (see figure 2);

splitting procedure (inherently included for receiving and splitting/passing portions of the digital timing control signal (Terr) to (472a, 472b) (see figure 4)) of passing at least a portion of the digital timing control signal;

procedure (comprising (472b)) (see figure 4) of processing the at least the portion of the digital timing control signal to produce the frequency control signal;

procedure (230a) (see figure 4) of providing the frequency control signal to a variable frequency generator (122a) of the AFC circuit, wherein the frequency control signal determines output frequency of the variable frequency generator.

-Claim 27 is rejected with similar reasons set forth for claim 6.

-Claim 28 is rejected with similar reasons set forth for claim 2.

-Claim 29 is rejected with similar reasons set forth for claim 4.

-Claim 30 is rejected with similar reasons set forth for claim 3.

Allowable Subject Matter

5. Claims 16-22 and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. References 20040120387 and 7133647 are additionally cited because they are pertinent to the claimed method and associated system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Phu
Primary Examiner
Art Unit 2611

Phuong Phu
01/25/07

PHUONG PHU
PRIMARY EXAMINER